Applications of memristive devices

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- Computer studies:
  - passive crossbar arrays
  - active crossbar arrays
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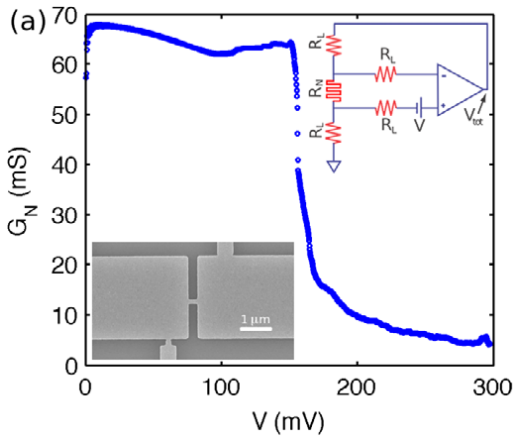
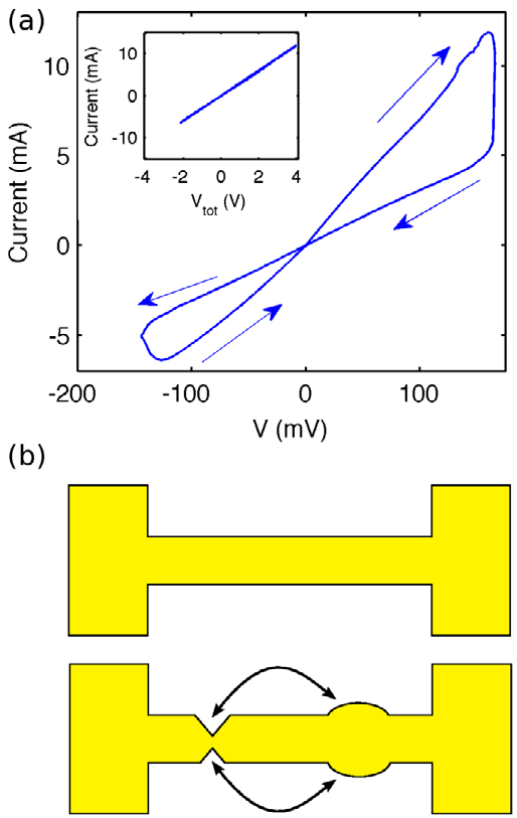
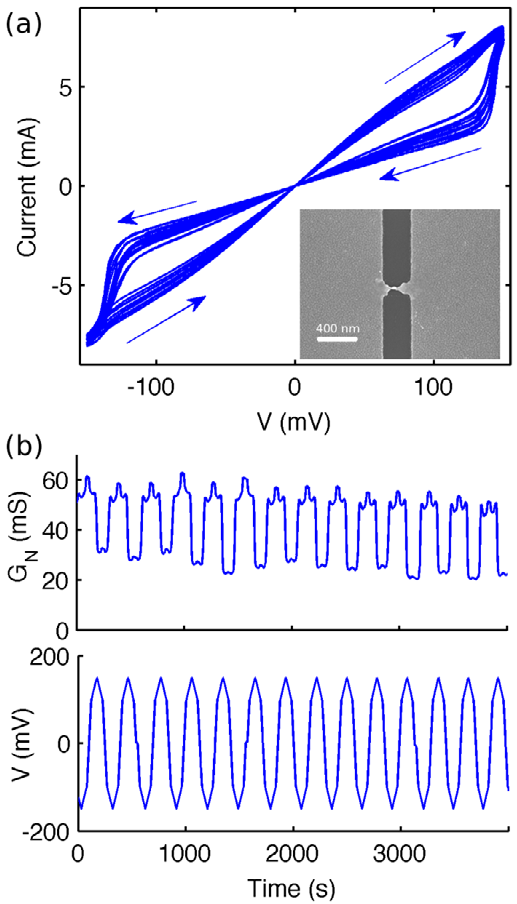
    $\Rightarrow$ Memcomputing
  - tricky examples: shortest-path problem, maze solution
  - Biological modeling

Electromigration [1]

New class of memristors: state variable = physical geometry

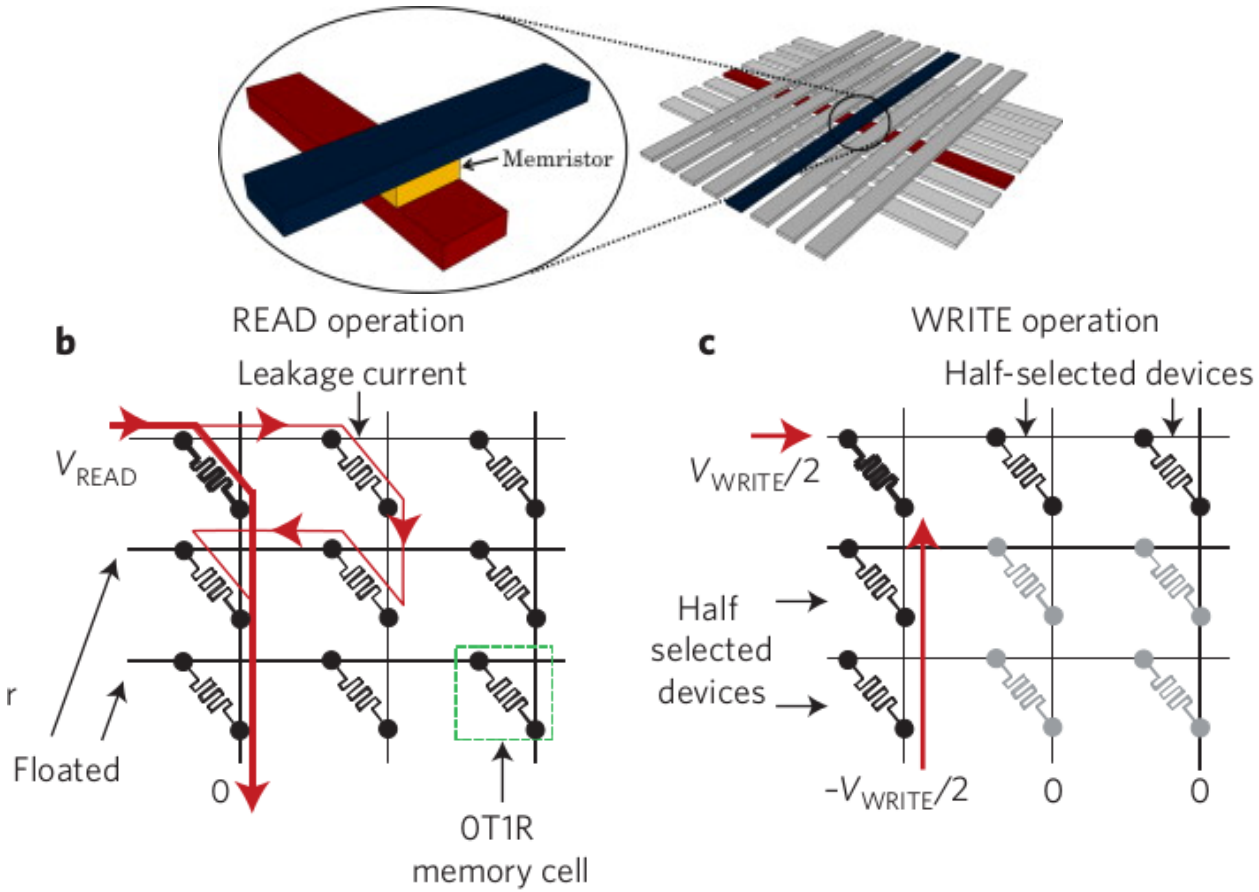






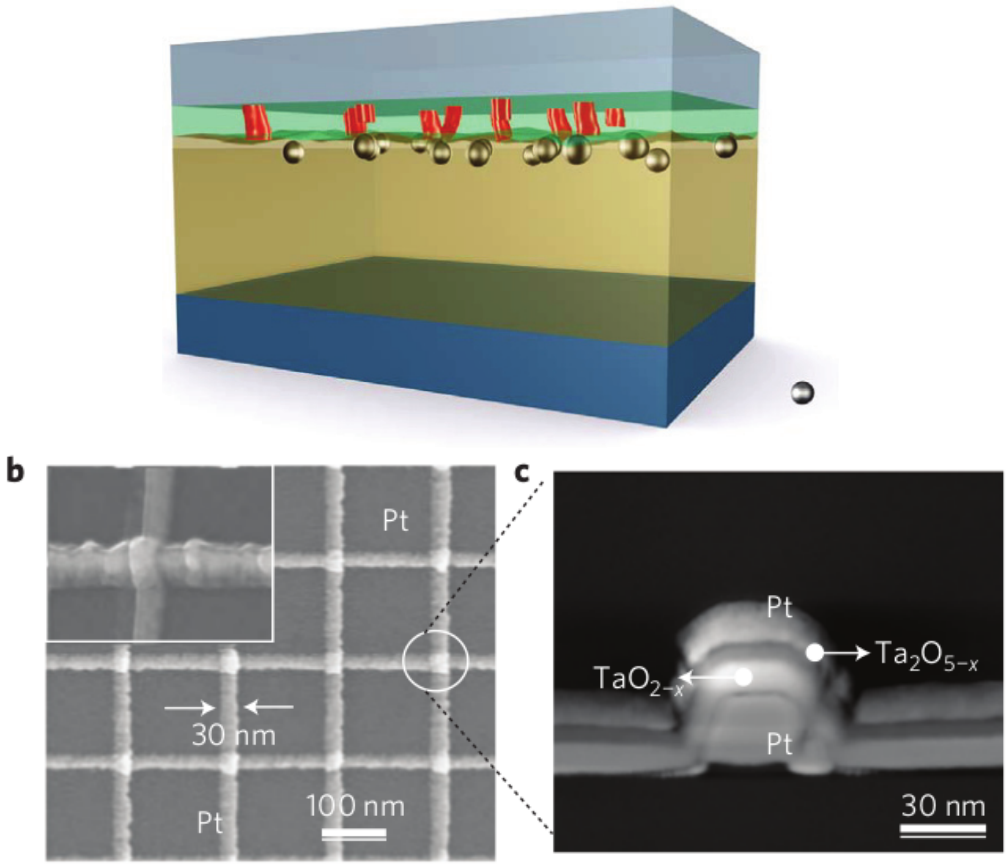
[1] S.L.Johnson et al., *Memristive switching if single-component metallic nanowires*, Nanotechnology, **21**, 125204 (2010)

Passive crossbar arrays [2]



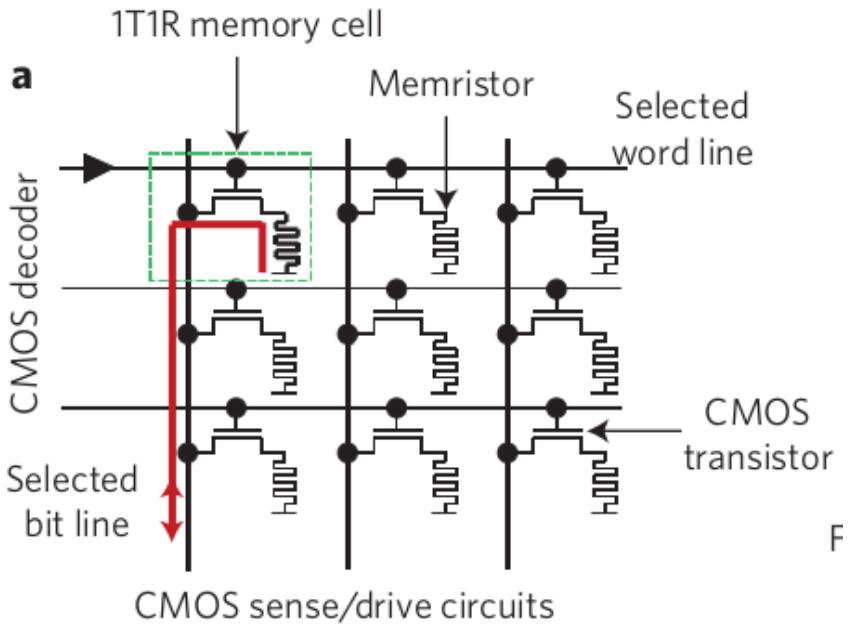
[2] J.J.Yang et al., *Memristive devices for computing*, Nature Nanotechnology, **8**, 13-24 (2013)

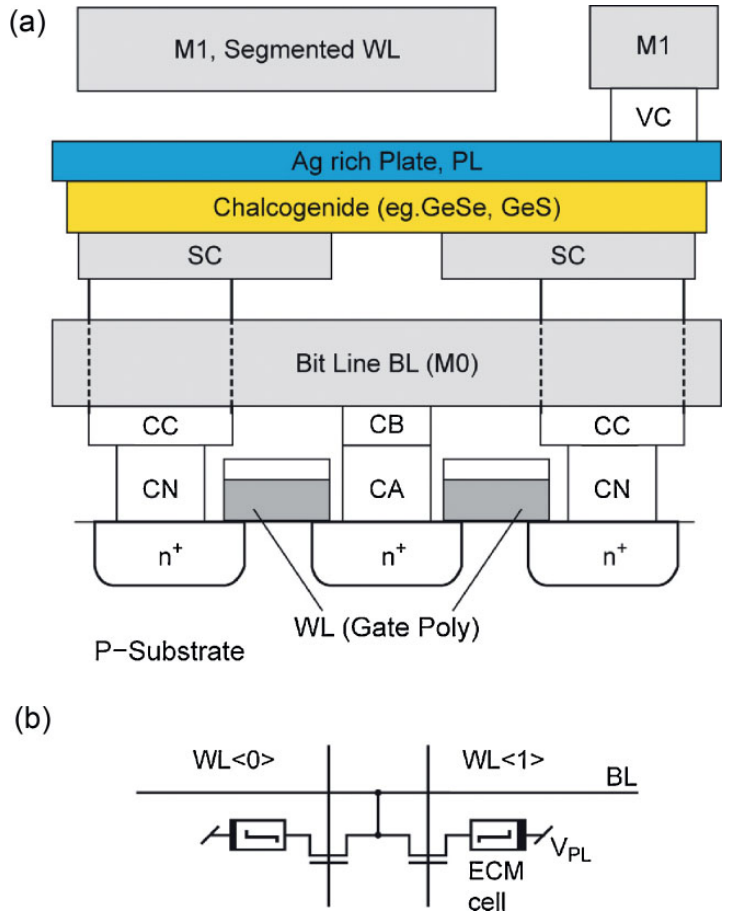
An example [3]



[3] M.Lee et al, *A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta2O5/TaO2 bilayer structures*, Nature Materials, **10**, 625 (2011)

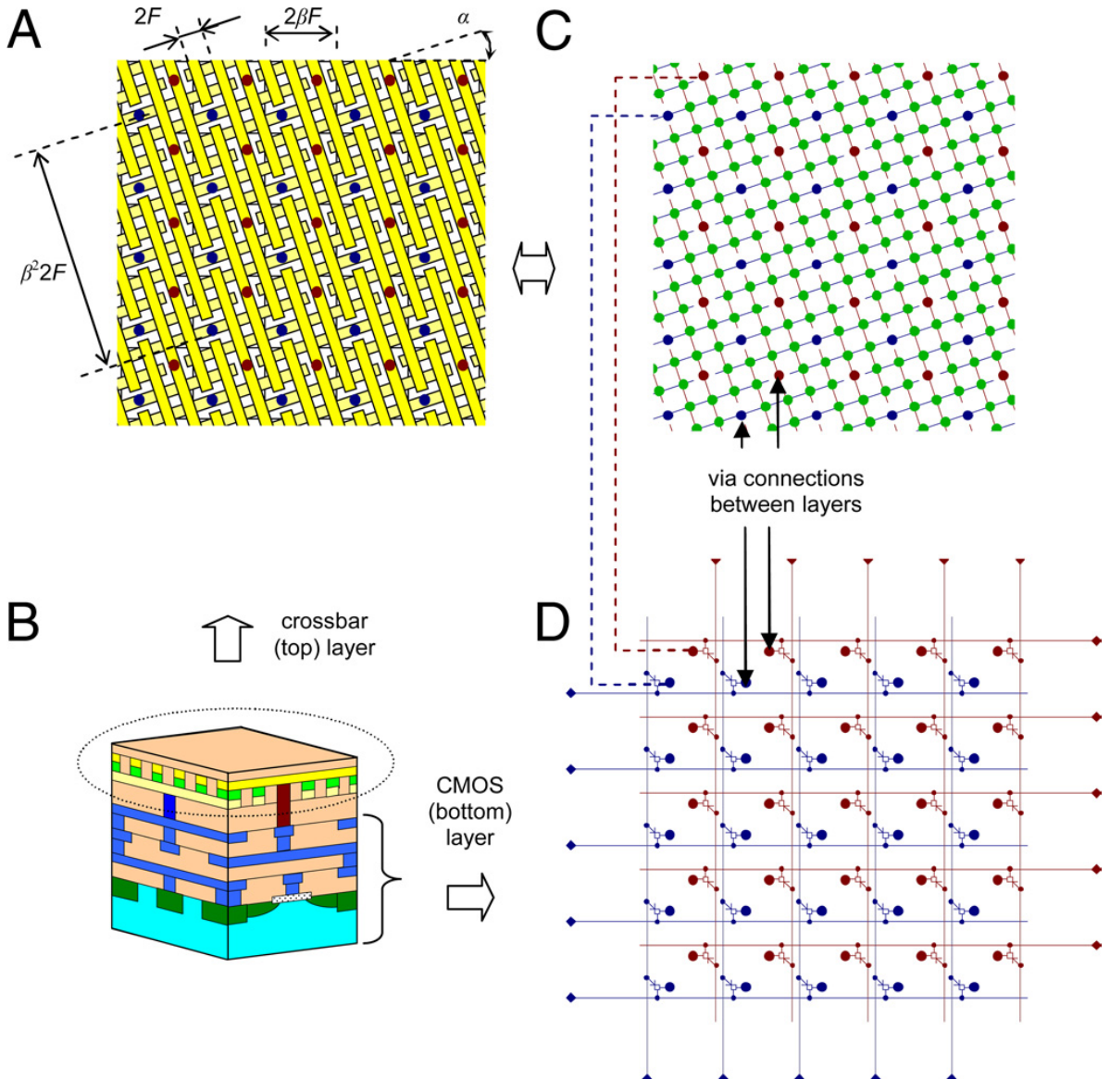
Active crossbar arrays [4]



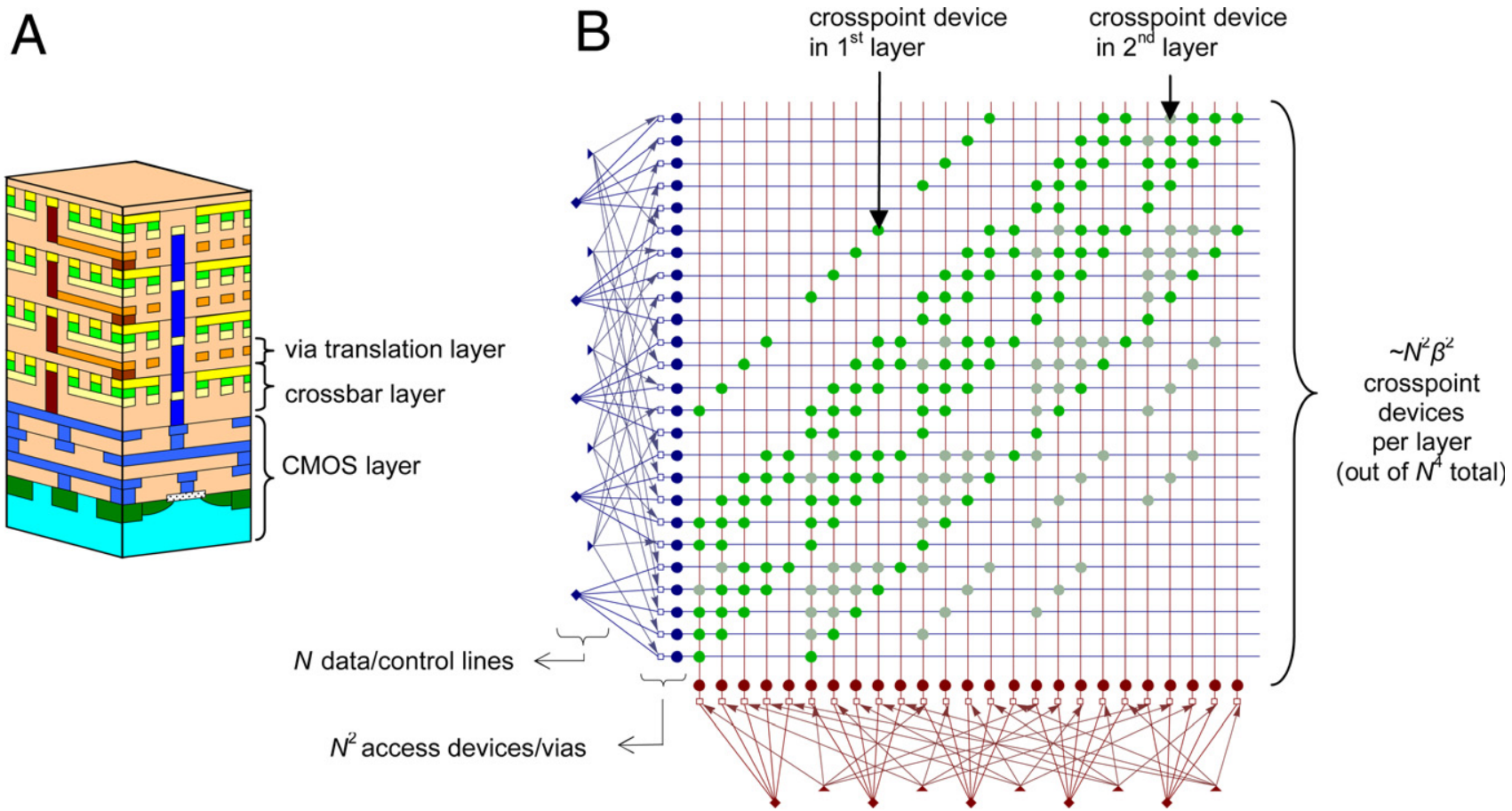


[4] S. Dietrich et al., *A Nonvolatile 2-Mbit CBRAM Memory Core Featuring Advanced Read and Program Control*, IEEE J. Solid-State Circuits, **42**, 839 (2007)

CMOS/memristor hybrid systems = CMOL

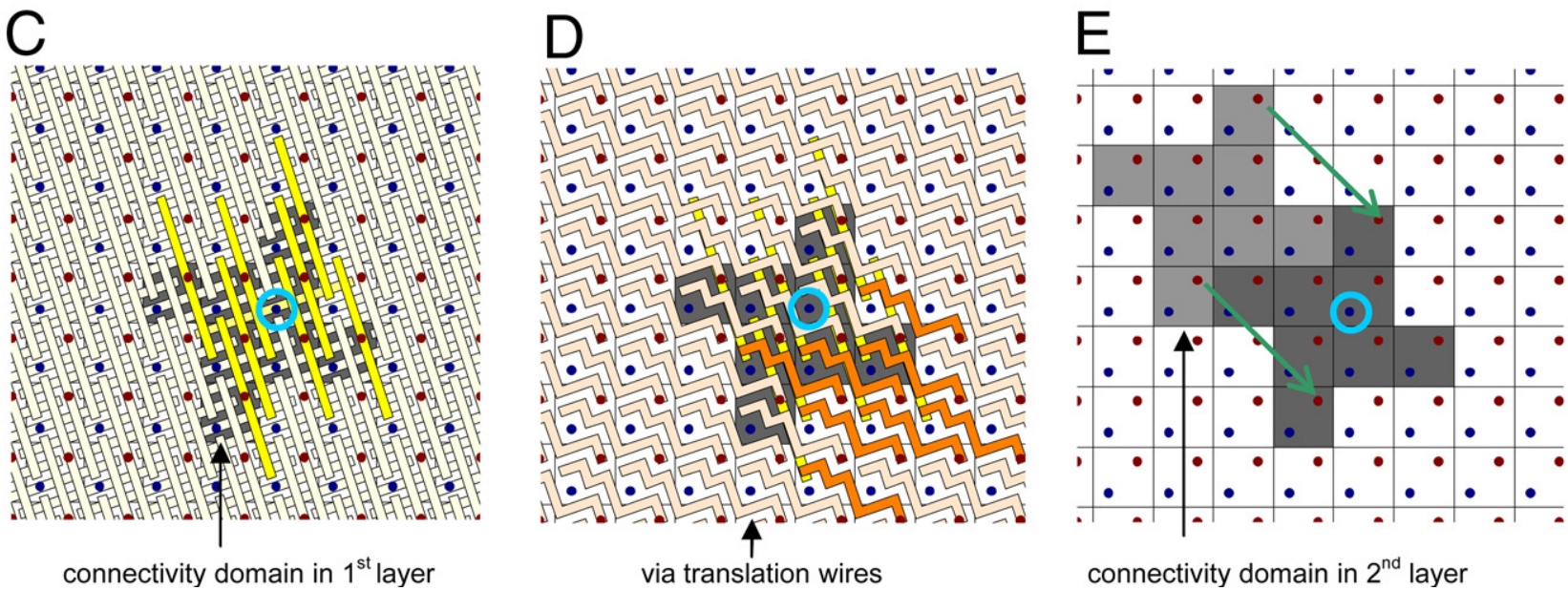


CMOL - 4 dimensions [5]



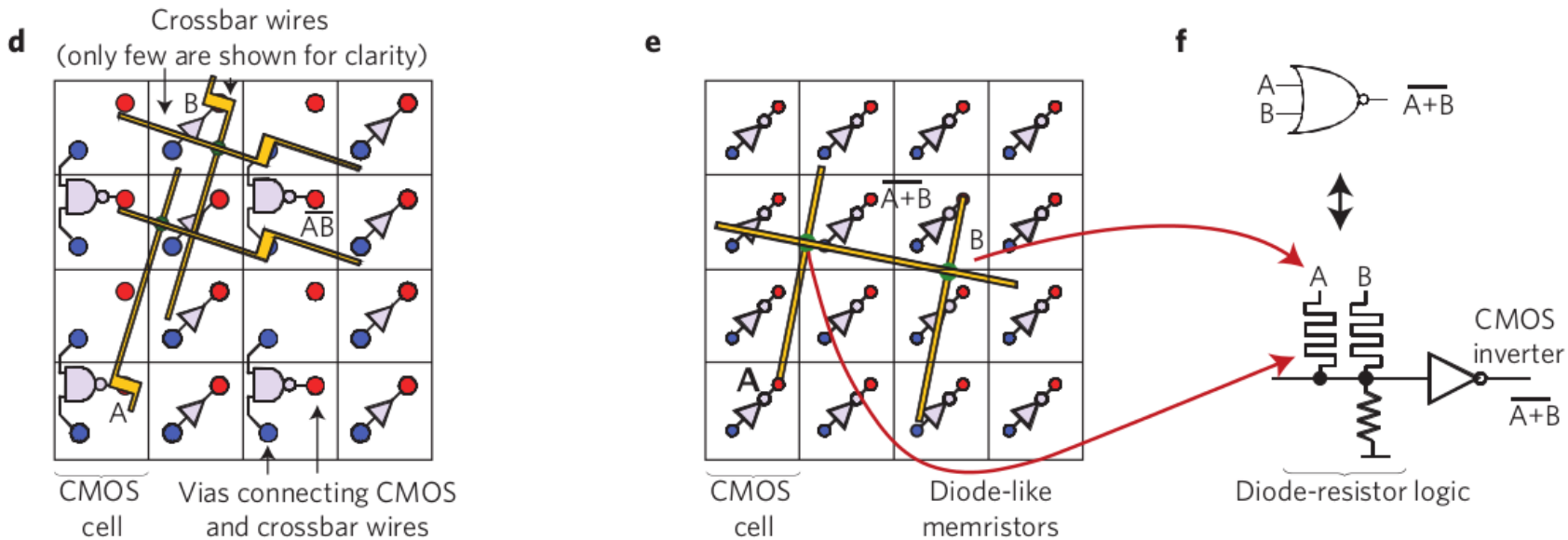
[5] D. Strukov and R. S. Williams, *Four-dimensional address topology for circuits with stacked multilayer crossbar arrays*, PNAS, **106**, 20155 (2009)

CMOL - 4 dimensions [5]



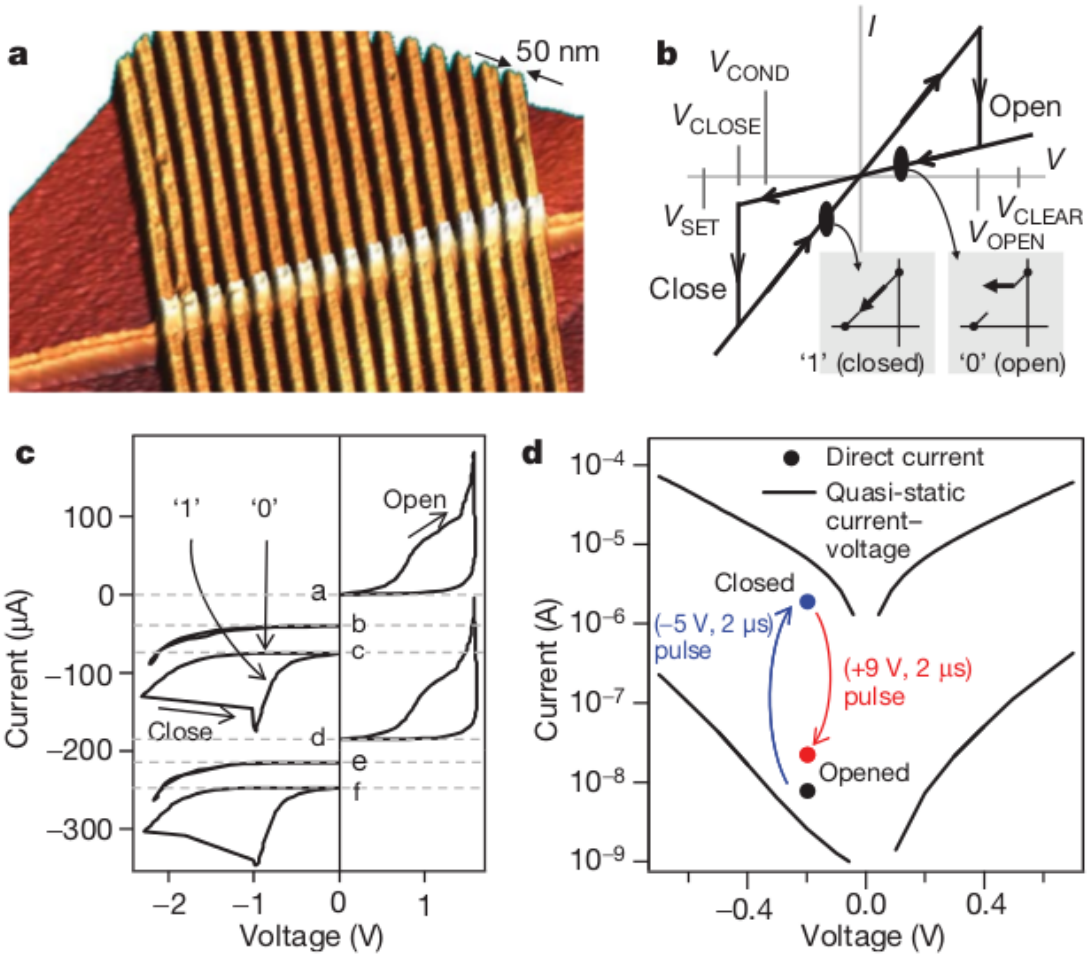
[5] D. Strukov and R. S. Williams, *Four-dimensional address topology for circuits with stacked multilayer crossbar arrays*, PNAS, **106**, 20155 (2009)

Programmable logic



Logic operations - IMP and NAND [6]

$Pt/TiO_2/Pt$
1x17 matrix

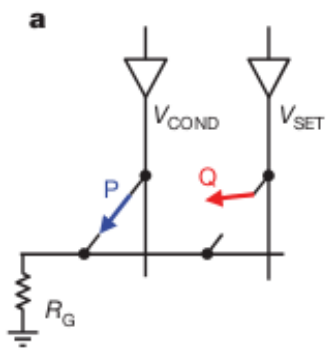


[6] J. Borghetti et al., *'Memristive' switches enable 'stateful' logic operations via material implication*, Nature, **464**, 8 (2010)

Logic operations - IMP [6]

Material implication

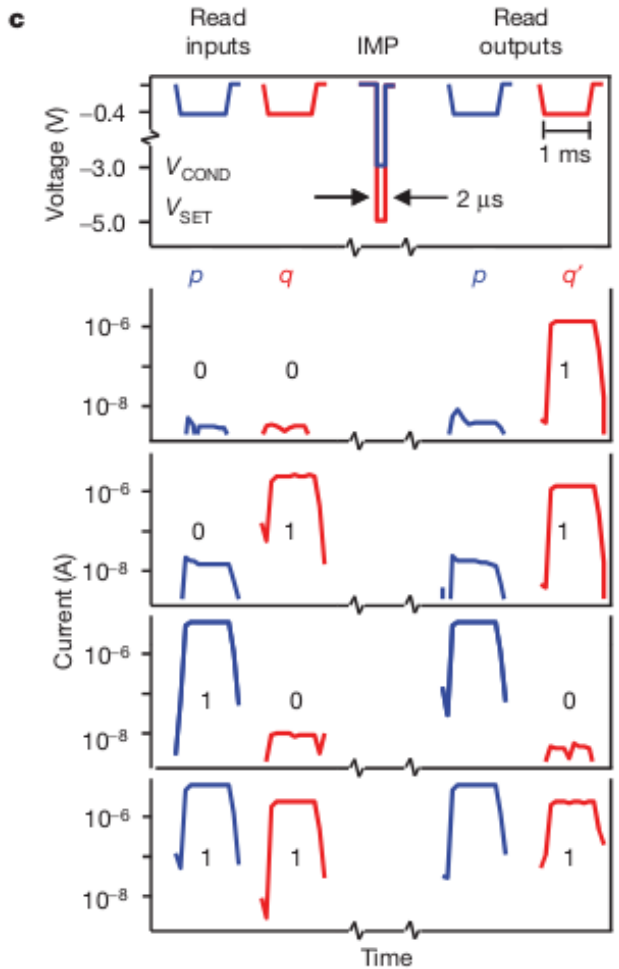
pIMPq=(NOTp)ORq
same as
'if p, than q'



b

$q' \leftarrow pIMPq$

In p	In q	Out q'
0	0	1
0	1	1
1	0	0
1	1	1



$$R_{ON} < R_G < R_{OFF}$$

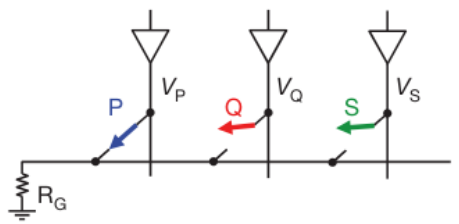
Logic operations - NAND [6]

NAND: universal, any Boolean logic operation can be constructed from an appropriate network of NAND gates

s ← pNANDq
in two steps:
s' ← pIMPs
s'' ← qIMPs'

a

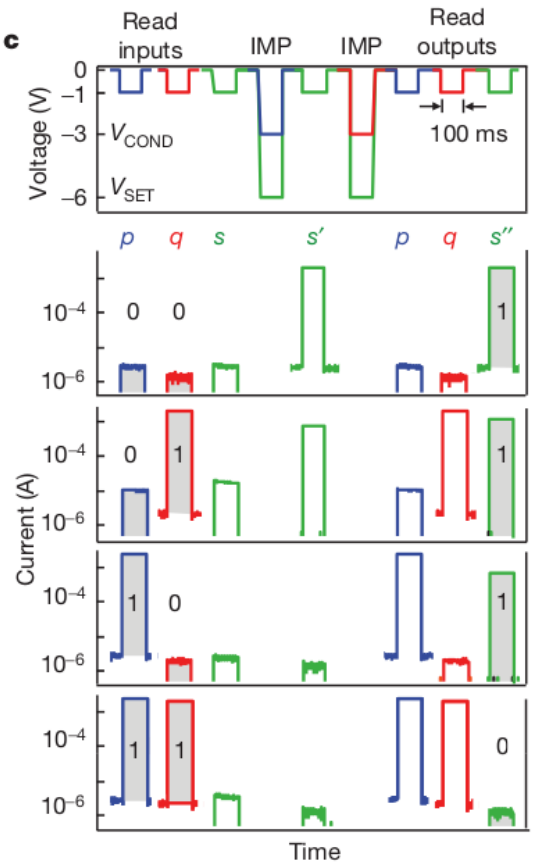
	Clocking voltages	
Step 1: $s = 0$		$V_S = V_{CLEAR}$
Step 2: pIMPs	$V_P = V_{COND}$	$V_S = V_{SET}$
Step 3: qIMPs	$V_Q = V_{COND}$	$V_S = V_{SET}$



b

Step 1	Step 2		Step 3				Steps 1, 2, 3		
$s = 0$	$s' \leftarrow p$IMPs		$s'' \leftarrow q$IMPs'			=	$s'' \leftarrow p$NANDq		
s	p	s	s'	q	s'	s''	p	q	s''
0	0	0	1	0	1	1	0	0	1
0	0	0	1	1	1	1	0	1	1
0	1	0	0	0	0	1	1	0	1
0	1	0	0	1	0	0	1	1	0

c



Memcomputing [7]

Aim:

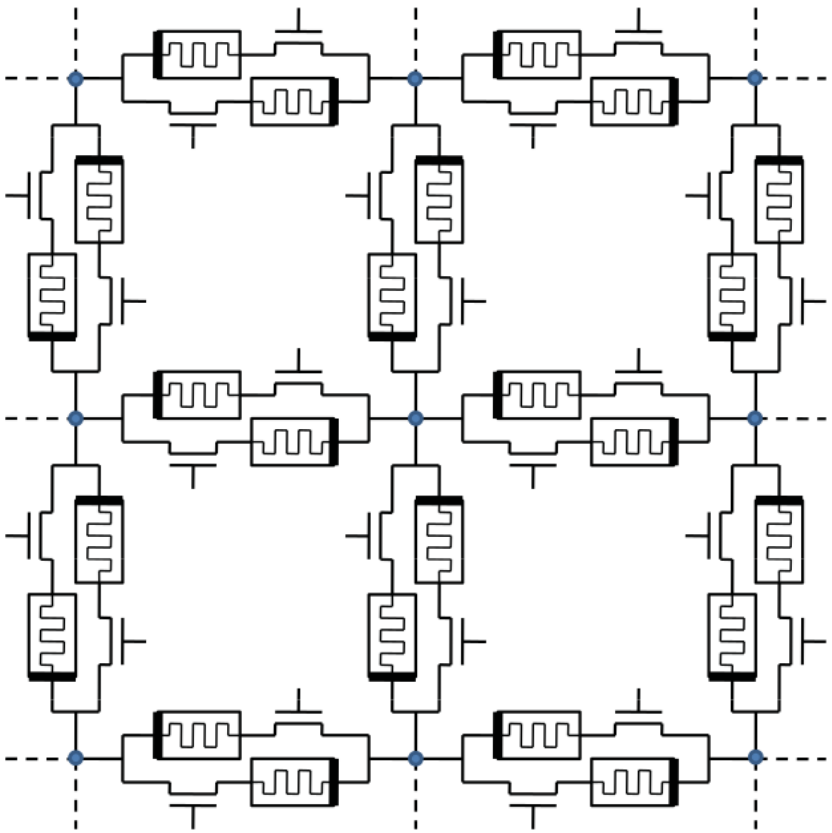
- Store and process information on the same physical platform
- massively-parallel computations

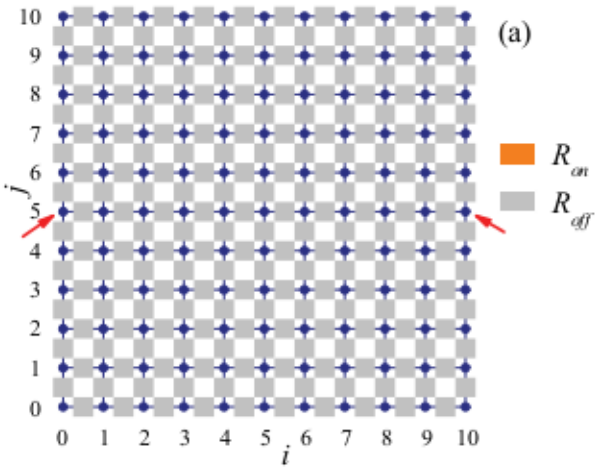
Criteria:

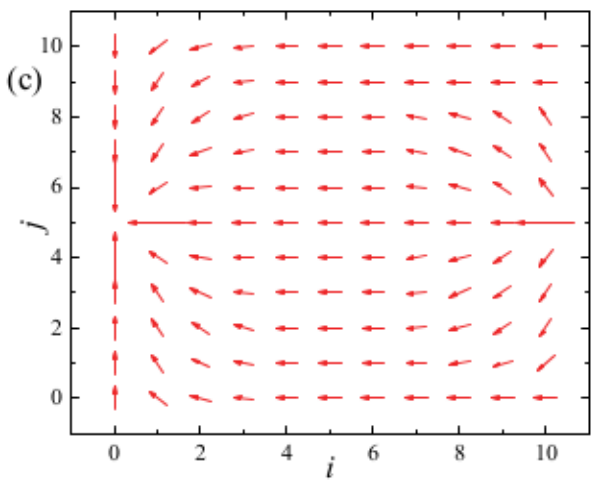
- scalable massively-parallel architecture with combined information processing and storage
- long information storage time
- the ability of initialization
- collective dynamics
- the ability of reading the results
- robustness against small damages and noise

[7] M.Di Ventra, arXiv:1200.4487v1 (2012)

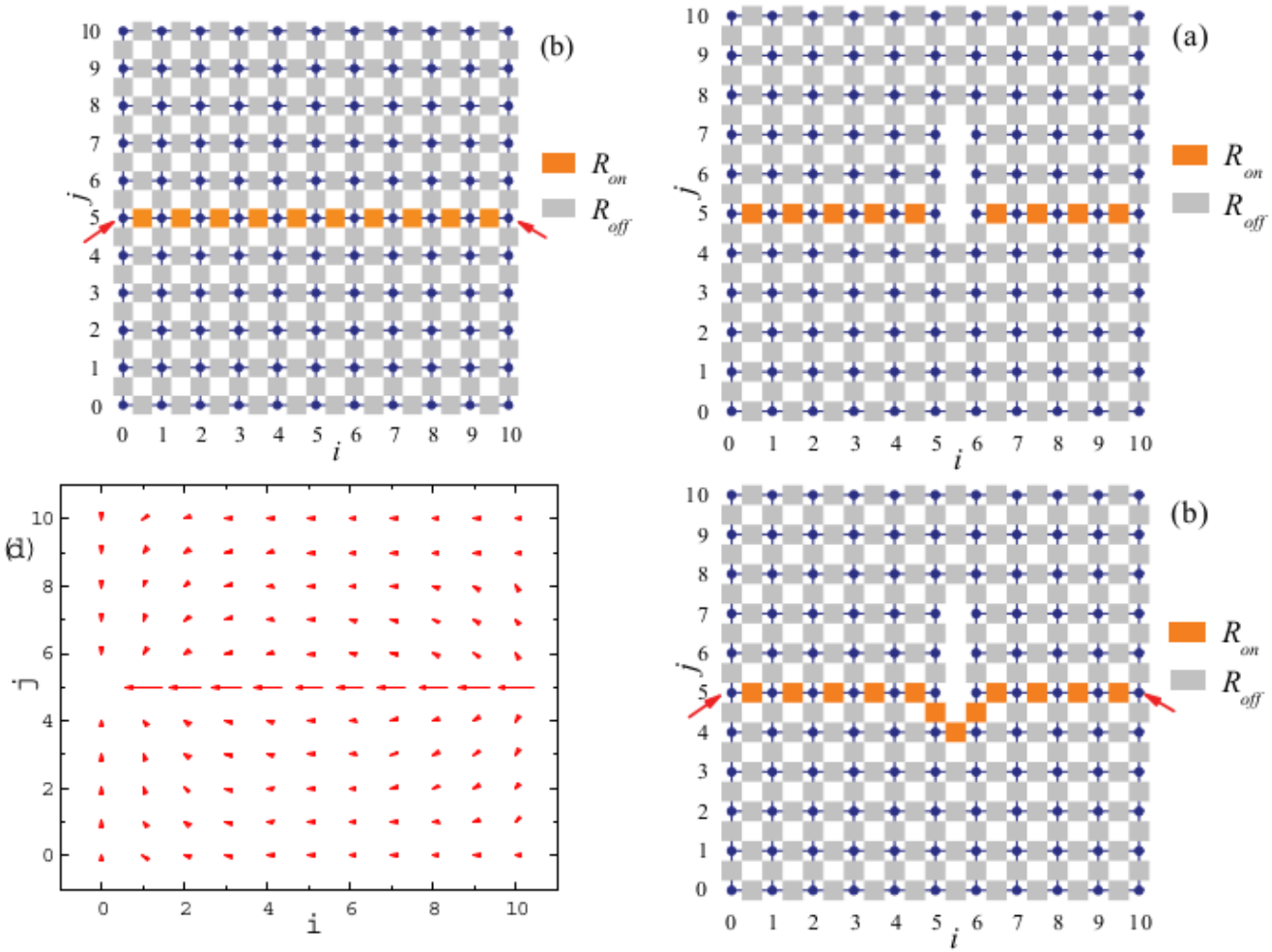
Examples - shortest-path problem [7]





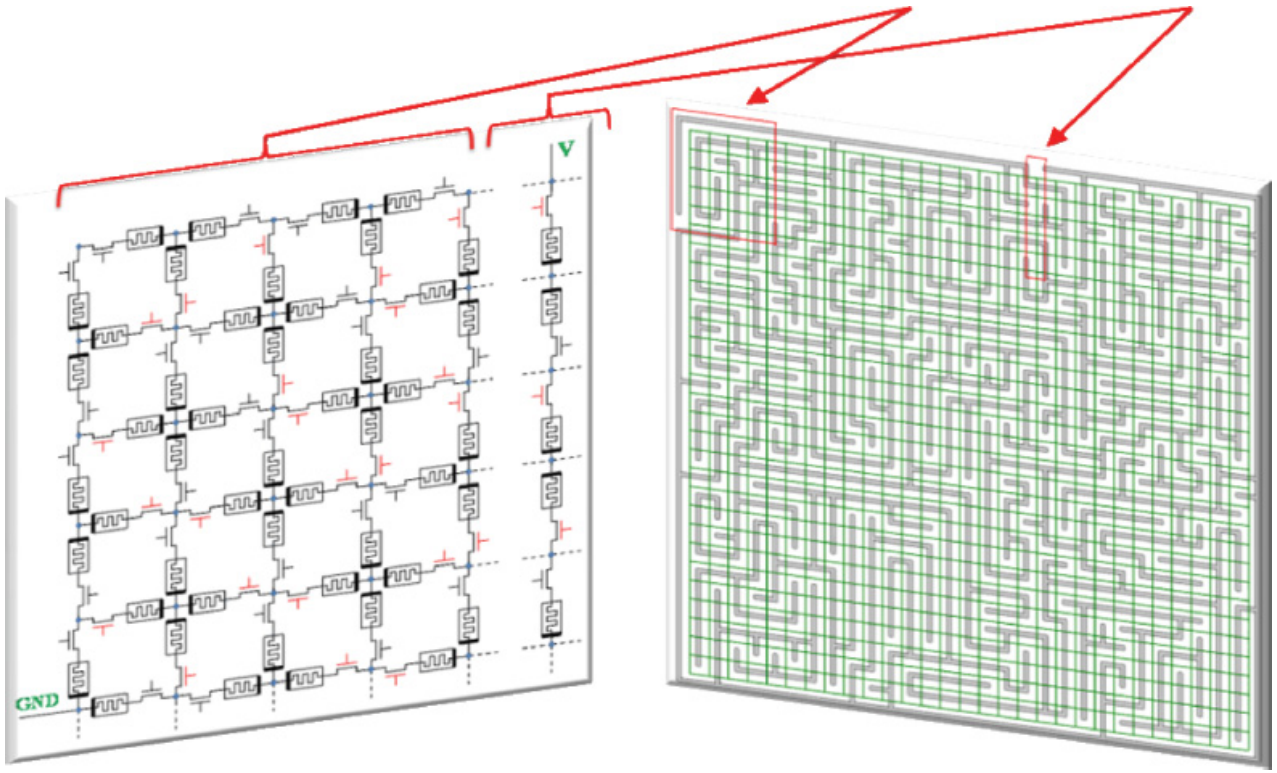


Examples - shortest-path problem [7]



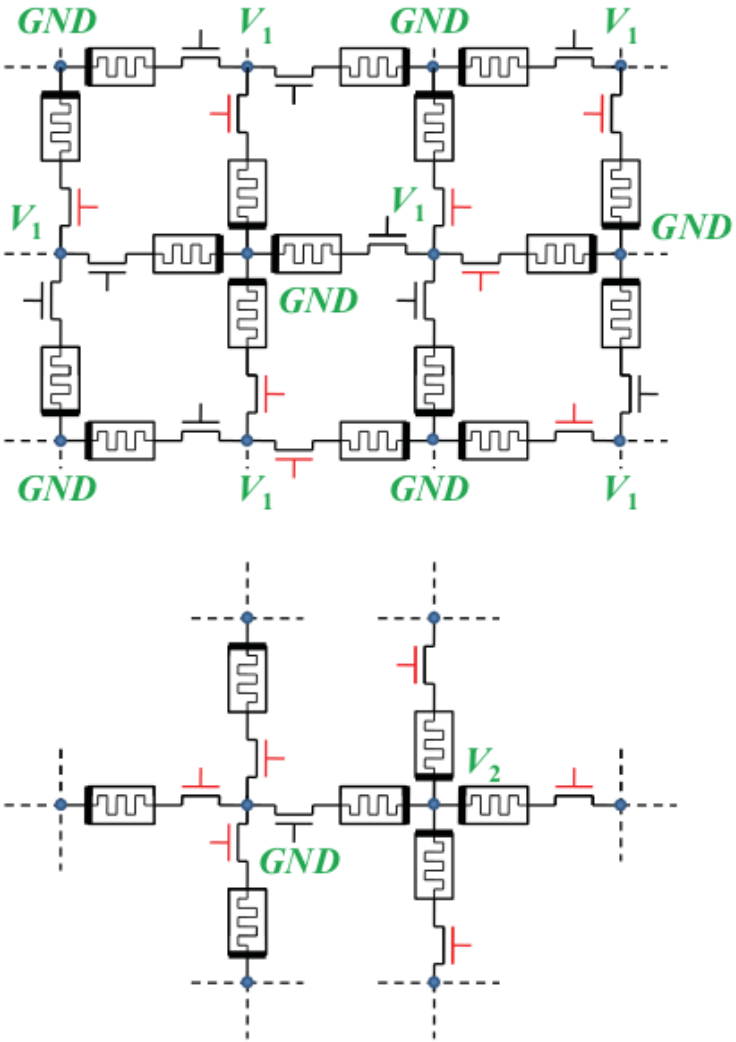
Examples - solving mazes [8]

Memristor processor requires only one step to find the maze solution.
Mapping:



[8] Y. V. Pershin and M. Di Ventra, *Solving mazes with memristors: A massively parallel approach*, Phys. Rev. E **84**, 046730 (2011)

Initialization and reading:



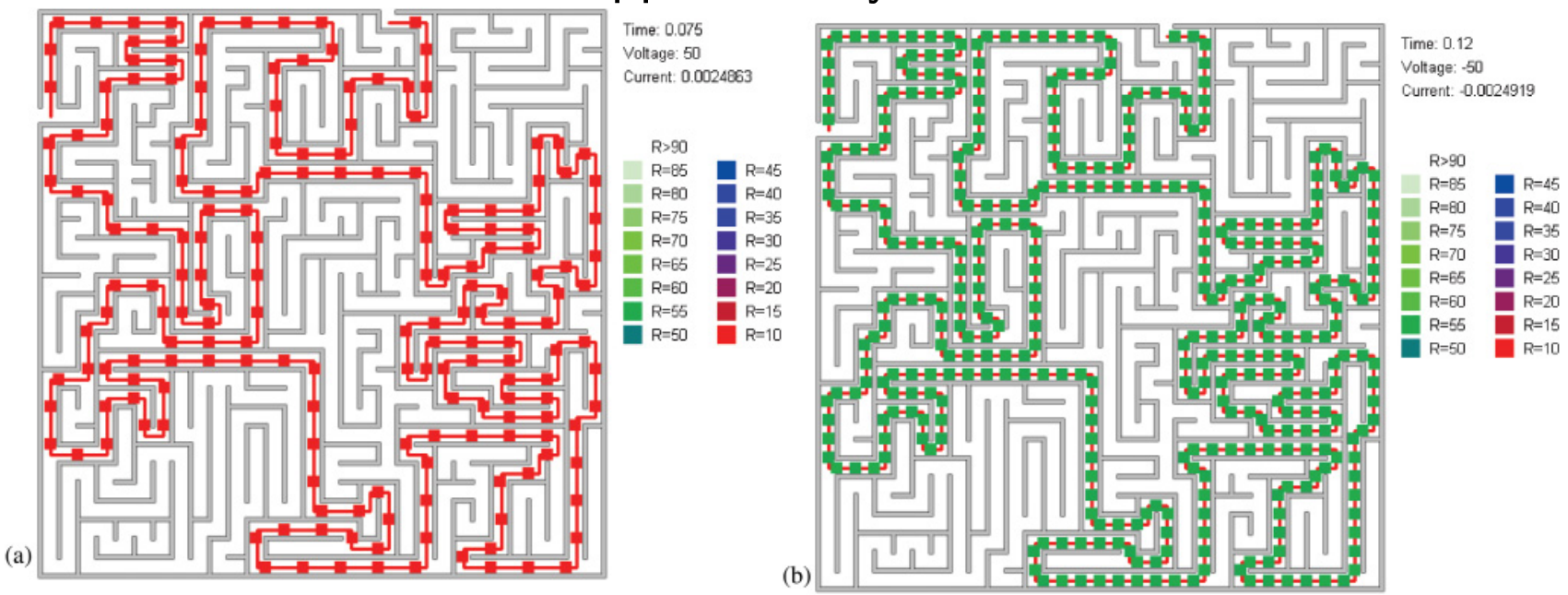
Numerical simulation:

$$R_{ij}^{M} = R_{ON}x_{ij} + R_{OFF}(1 - x_{ij})$$

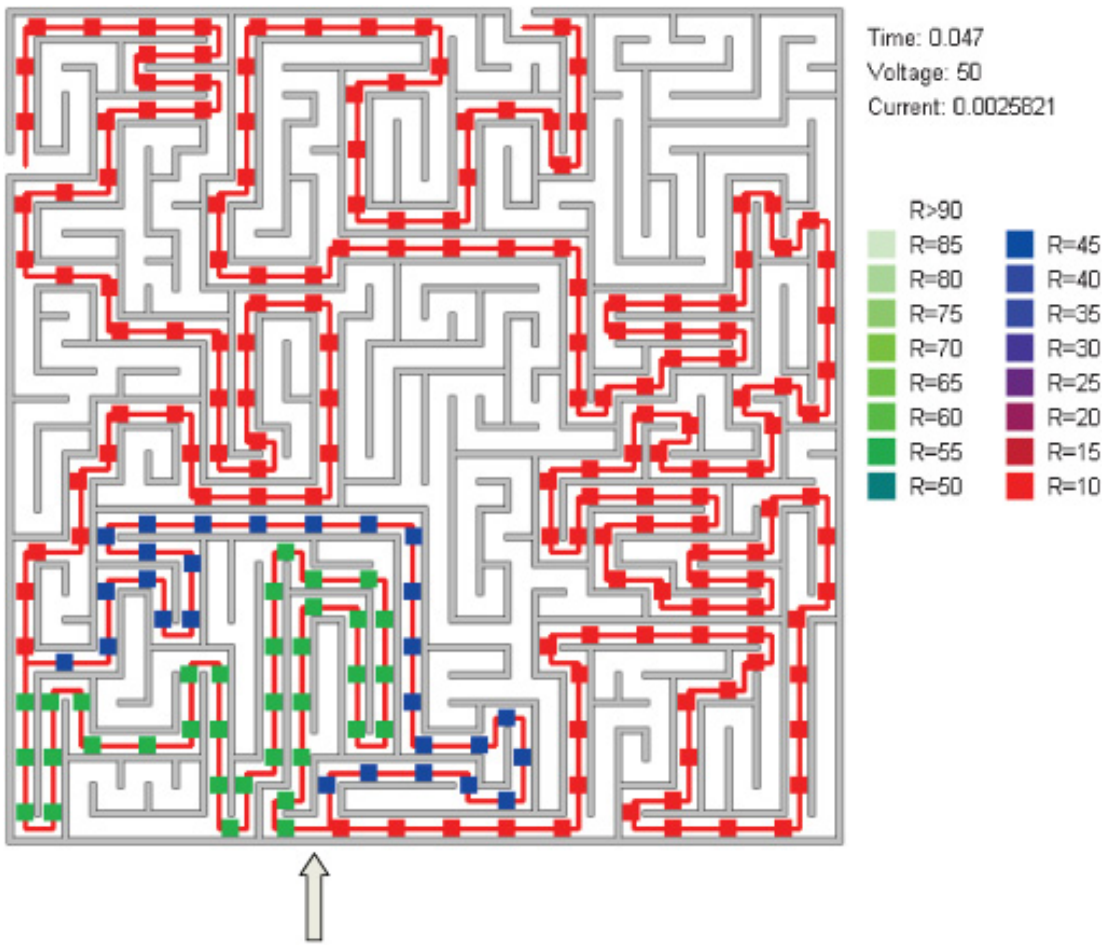
$$\frac{dx_{ij}}{dt} = \alpha I_{ij}(t)$$

Results - single-path maze

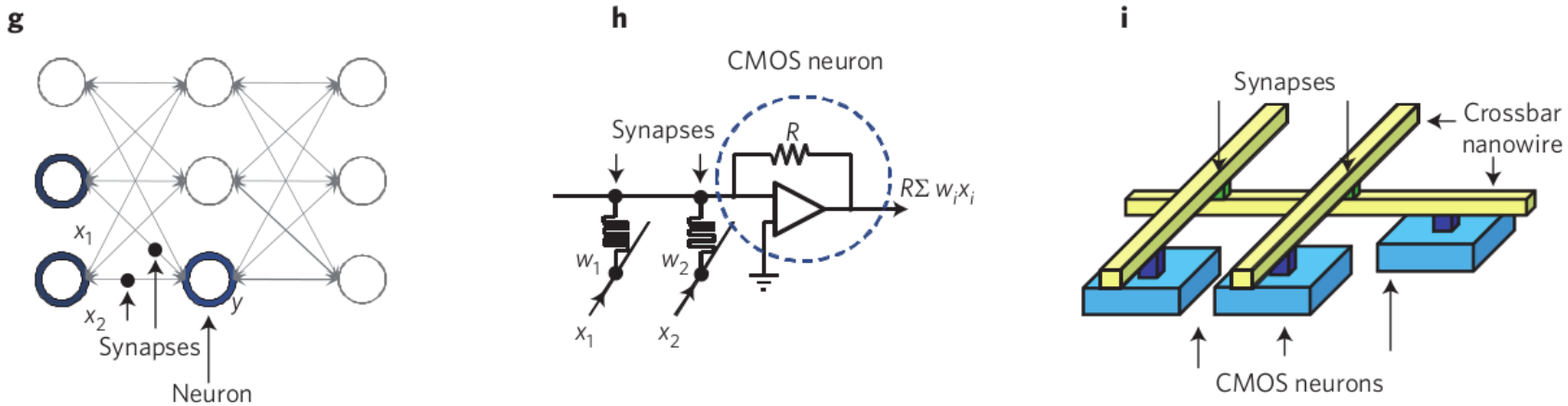
There is a movie in the supplementary!



Results - multiple-path maze



Biological modeling



Summary of the used articles I

1. Electromigration: S.L.Johnson et al., *Memristive switching if single-component metallic nanowires*, Nanotechnology, **21**, 125204 (2010)
2. Great references: J.J.Yang et al., *Memristive devices for computing*, Nature Nanotechnology, **8**, 13-24 (2013)
3. Passive crossbar: M.Lee et al, *A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta2O5/TaO2 bilayer structures*, Nature Materials, **10**, 625 (2011)
4. CMOS hybrid: S. Dietrich et al., *A Nonvolatile 2-Mbit CBRAM Memory Core Featuring Advanced Read and Program Control*, IEEE J. Solid-State Circuits, **42**, 839 (2007)

Summary of the used articles II

5. CMOL: D. Strukov and R. S. Williams, *Four-dimensional address topology for circuits with stacked multilayer crossbar arrays*, PNAS, **106**, 20155 (2009)
6. Logic operations: J. Borghetti et al., *'Memristive' switches enable 'stateful' logic operations via material implication*, Nature, **464**, 8 (2010)
7. Memcomputing and shortest-path: M.Di Ventra, arXiv:1200.4487v1 (2012)
8. Maze solution: Y. V. Pershin and M. Di Ventra, *Solving mazes with memristors: A massively parallel approach*, Phys. Rev. E **84**, 046730 (2011)

Interesting articles for future reading

- Kim et al., *A Functional Hybrid Memristor Crossbar-Array/CMOS System for Data Storage and Neuromorphic Applications*, Nano Letters, **12**, 389-395 (2012)